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DV Meter

500 Mk II

MP MASTER
MA24475

Weir Electronics Limited

DURBAN ROAD · BOGNOR REGIS · SUSSEX · ENGLAND

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D V Meter
500 Mk II

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Weir Electronics Limited

DURBAN ROAD · BOGNOR REGIS · SUSSEX · ENGLAND
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1. INTRODUCTION

The DV Meter 500 Mk II has been designed to a 'value for money' philosophy to give a high performance/cost ratio. The novel circuits employ readily available components mounted on printed wiring boards to give high operational reliability. The number of preset controls has been reduced to a minimum to simplify setting up and test procedures and thereby minimise manufacturing costs.

The Digital Voltmeter consists of a voltage-to-number converter driving decade counters. The problems of stability in the voltage-to-number converter have been overcome by employing similar circuits for timing and voltage-to-frequency conversion, and these circuits are coupled both thermally and electrically so that any drift in one will be reflected in the other. Thus, the relative drift is extremely small.

The input voltage to be measured is first applied through an attenuator to a transistor-chopper operational amplifier which gives high common mode rejection and high input impedance. The output from the amplifier is a current proportional to the input voltage, and this is used as the charging current for an integrating circuit which produces a number of output pulses proportional to the voltage being measured. These pulses are then counted in a three decade counter, and the carry from the most significant decade operates a single digit display to give the instrument an overall range from zero to 1100.

The instrument is small, light and portable. It is robustly built and protected against overload up to 1000 volts on the input terminals. It will therefore be eminently suitable for use in schools and colleges as well as in laboratories and production test departments. The instrument is contained in an aluminium case clad with light fawn p.v.c. and the front panel and front trim are of satin anodised aluminium.

2. SPECIFICATION

Ranges (Push button selected)

Range	Sensitivity	Input Resistance	
0 - 1·100V	1mV	1MΩ	±2%
0 - 11·00V	10mV	10MΩ	
0 - 110·0V	100mV	10MΩ	
0 - 1000V	1V	10MΩ	

Any range may be specially scaled by adding one external resistor of appropriate value.

Accuracy

±0·2% of full scale, ±one least significant digit.

Calibration

The internal calibration voltage is derived from a low temperature coefficient zener diode having a stability of ±0·001% per year at normal temperatures.

Temperature Range (Ambient)

0° to 50°C Storage
+10° to 35°C Operating
Warm-up time 30 mins for maximum accuracy

Attenuators

Attenuation ratio accurate to ±0·05% at normal ambient temperatures. Long term stability 0·025%. An internal preset trimming potentiometer is used to offset this drift by comparison with an external voltage standard. Metal oxide attenuator resistors are employed, having a temperature coefficient of <50PPM/°C.

Common Mode Rejection

With 1KΩ unbalance in either lead

dc	>120dB
ac 50Hz	>60dB (1V and 10V ranges only)

Maximum common mode voltage to chassis should not exceed 1000 volts peak.

Series Mode Rejection

ac50Hz >36dB

Input

The input circuit is isolated from chassis by >100MΩ and 100pF from either terminal to ground.

Input Overload

Voltages up to 1000V dc will not damage the instrument irrespective of the range in use.

Input Polarity

Polarity may be reversed by a push button switch, which also operates the positive terminal neon indicator lamps.

Operating Modes

Reading repetition rate variable from a maximum rate of 3 per second to infinity. 'Single Shot' and 'Hold' measurement is effected by use of the 't' control. Maximum digitising time <250mS.

Readout Display

Four windows comprising three neon decade number tubes with associated neon lamp decimal point indicators preceded by a neon figure '1' lamp.
A polarised light filter eliminates reflection and enhances the display contrast in high ambient light conditions.

Power Unit

Selected Transformer Taps:

110V	+6 −12%	50-60Hz	20W
115V	+6 −12%	50-60Hz	20W
220V	+6 −12%	50-60Hz	20W
240V	+6 −12%	50-60Hz	20W

The supply is fed via a captive three core cable. A 0·5amp fuse is fitted in the supply line.

Dimensions

10·5" wide x 3·75" high x 13·25" deep (26·7 x 8·6 x 33·7cm)

Weight

7lbs (3·5Kg)

Finish

Light fawn p.v.c. clad aluminium with satin anodised aluminium trim and front panel.

3. OPERATING INSTRUCTIONS

Initial Adjustments

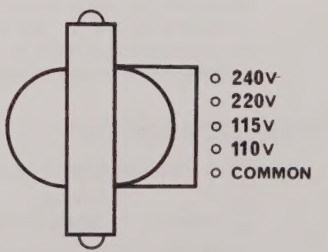
a)Transformer Tap Selection.

The instrument is normally dispatched with the power transformer tappings adjusted for 240V ac supply. If this does not suit the local line voltage, the wiring to the transformer must be modified.

Remove the top case assembly as described in Section 5.

Rewire the transformer tappings to suit the local line voltage.

Replace the power supply board and top case assembly.



b) Power Plug.

A suitable power plug must be fitted to the instrument power cable. The wires are colour coded as follows:
Red-Line; Black-Neutral; Green-Ground.

Control Functions

a) General.

The control adjustments described in the ensuing paragraphs should not be attempted until the instrument has been switched on for 30 minutes to reach thermal stability. (see Operating Sequence, below).

b) 'Set 005'

The preset 'Set 005' control is provided to compensate for any small drifts which may occur while the digital voltmeter is being used. The mode is selected by pushing the right hand push button, and the correction is made by adjusting the screwdriver control immediately below the button until the display indication is 005.

c) 'Set 912'

The preset 'Set 912' is provided to permit the voltmeter accuracy to be checked and, if necessary, reset at the commencement of each set of readings. The left hand push button marked 'Set 912' is pressed and the screwdriver control below it is adjusted until the digital display indication equals the number engraved against the control.
NOTE: The number given in the text above is typical, but a different number, depending on the internal zener reference voltage will be found on each instrument.

d) Range Controls

The range controls are the four push buttons in a vertical line immediately to the left of the display. They set the sensitivity of the instrument and determine the maximum voltage which may be displayed. The range selected is indicated automatically by the position of the decimal point in the display.

e) Input Terminals

The signal to be measured is connected to the input terminals at the bottom of the control panel. The positive side of the voltage being measured should connect to the positive terminal, which is indicated by a glowing neon situated immediately above the terminal. The polarity of the input terminals may be reversed by pressing the polarity button, which is the centre one of three situated above the terminals.

f) Sampling Time 't'

The digital voltmeter samples the voltage to be measured repetitively and displays the result for the period between samples. The repetition rate is sufficiently slow to ensure a readable display, but if there is any fluctuation of the input voltage, instability of the last digit may occur. This may be restricted by slowing down the sampling time, or in the ultimate, restricting to one sample only. In this condition, with the sampling time control 't' turned to the left, the voltmeter takes one measurement only and displays the result until the sampling time control is returned to a position giving repetitive sampling.

Operating Sequence

This information is provided as a guide to users who are unfamiliar with digital instruments.

a) Connect the instrument to the ac supply line and allow it to warm up for 30 minutes to reach thermal stability.

b) Turn the sampling time control 't' from left to right to initiate a reading.

c) Select the range required, and when in doubt, select a range less sensitive than the one required.

d) Push the 'Set 005' button and check that the indication is 005; if necessary, adjust the preset control.

Note: When checking or adjusting 'Set 005' and 'Set 912', link the 'low' input terminal to earth.

e) Press the 'Set 912' button and check that the reading corresponds with the figure on the front panel below the 'Set 912' button; if necessary, adjust the preset control.

f) Connect the voltage to be measured to the input terminals and observe the reading on the digital display; if the reading is less than 110 in the last three windows, select the next most sensitive range.

g) If the reading remains all at zero, reverse the polarity of the input terminals by pushing the 'polarity' button.

h) If the reading is 1100, select the next less sensitive range.
1400

Operating Notes

When operating on the most sensitive range of the instrument, the extreme right hand digit will change for changes of input voltage as small as 1 millivolt. Special precautions must therefore be taken to ensure stable readings on this range. The measured voltage must be firmly connected to the instrument.

When long leads are used to connect the voltmeter to the voltage being measured, interference voltages may be introduced in both leads;this is termed common mode interference and the voltmeter will provide automatic rejection up to 60dB of d.c. common mode signal. This means that on the one volt range, one volt of common mode interference at 50Hz will introduce an error of less than one digit in the most sensitive window, i.e., 1 millivolt.

Interference signals may also be introduced into one signal line only, so that they appear in series with the signal to be measured. This is called series mode interference,and input filtering combined with the chopping frequency of the d.c. amplifier, will give 36dB of series mode rejection to 50Hz signals.

When measuring signals from thermocouples, resistance thermometers, and other forms of transducer, it may be desirable to scale the output reading directly to the parameter being measured. This may be done by inserting an accurate attenuating resistor in series with the input terminal of the voltmeter, so that the input signal to the ranging resistor is attenuated to a suitable level.
e.g. If the output from the transducer is 13 volts for a load of 10lbs, insert a 3MΩ resistor in series with the input voltage. Then at full load on the transducer, the input voltage will be attenuated to 10 volts at the input terminals of the instrument, which will indicate directly in pounds weight.

While this method can be used for scaling the instrument, it does not provide linearisation and any non-linearities in the transducer law will exist in the voltmeter readings.

4. TECHNICAL DESCRIPTION

Principles of Operation

The block diagram, Fig. 1, shows the method of operation of this instrument. The voltage to be measured is converted to a number of pulses, the pulse repetition frequency being proportional to the input signal. These pulses are counted for a period determined by a timing circuit and the final count is shown on the digital display.

In similar instruments, great care has to be taken to obtain accuracy and stability in both the voltage-to-frequency converter and the timing circuit. However, in this instrument, both circuits are of the same basic configuration and are closely coupled both thermally and electrically so that any variations in ambient temperature, or in supply rails, will have an equal effect on both circuits. Thus, although the individual stabilities of the two circuits are not high, their relative stability is excellent, permitting an outstanding performance from this low cost instrument.

The input signal enters the instrument through an attenuator operating in decade steps. This signal is passed through a dc operational amplifier which provides a constant current, proportional to the input voltage, for the voltage-to-number converter. Negative feedback around the dc amplifier ensures its stability and an offset voltage fed to its summing junction permits the zero of the instrument to be set. Pulses from the voltage-to-number converter drive three decade counters in cascade and the outputs from the counter drive the digital display directly.

The sampling sequence is as follows: An output from the sampling generator triggers the gate bistable which removes inhibit signals from the voltage-to-number converter and from the timing circuit. Pulses from the voltage-to-number converter than pass to the counter, and the timing circuit commences to operate, driven by a constant current derived from the reference voltage. When the timing circuit has completed its cycle, it resets the gate bistable, inhibiting the operation of the voltage-to-number converter. The output from the three decade counter is then displayed by the digital display until the next signal from the sampling generator.

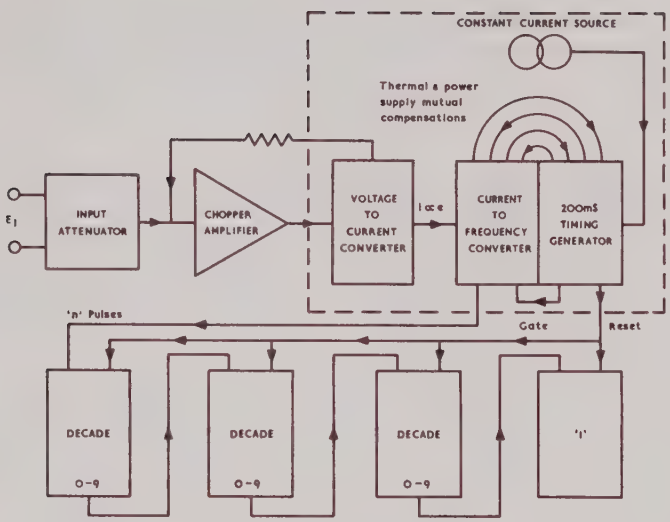


Fig. 1. Block Schematic Diagram

The Switch and Neon Circuits

The circuits associated with the input attenuator, the mode select switching, and the circuit for the most significant digit of the display are all shown on one circuit diagram, Fig. 2. The function of each of the switches will be described in turn and the neon indicator circuit will be left until last.

The 'Set 912' switch, SA, has three sets of operating contacts. The first, SA4, breaks the return to zero volts path of the input attenuator, to prevent any loading of the standard calibration signal. The second, SA2, switches the standard calibration signal which appears across R11 and R12, to the input of the operational amplifier through R19 and R7. The third, SA3, opens to include R7 in the signal line.

The polarity switch, SB, has three sets of operational contacts. Two of these, SB1 and SB3, are arranged as a double pole change-over switch which may connect either of the front panel input terminals to the input attenuator, the other terminal being connected to the zero volts line. The third contact, SB4, connects the zero volt line to the neon which indicates the positive terminal.

The 'Set 005' switch, SC, has three sets of working contacts. Two sets, SC2 and SC3, work in series with contacts of SA and perform the same functions. The third set, SC4, connects a very small reference voltage which appears across R12, to the input of the operational amplifier through R19, to give a display, when the digital voltmeter is correctly set, of 005.

The range selector switches, SD, SE, SF, and SG, connect the voltage to be measured to various points on the input attenuator chain, and adjust the attenuation to suit the range selected. The operation of the various switches is as follows:

a) The 1 volt range is selected by SD. The input signal is connected through SD4, SA2, SC4, R19 and R7, directly to the input of the operational amplifier. SD3 disconnects the attenuator return paths through R16 and R17, from the zero volt line, while SD1 connects the neon N4 to the zero volt line to provide a decimal point between the first and second digits of the display.

b) The 10 volt range is selected by SE. The input signal is connected to the input attenuator through SE4 at the junction of R8 and R9; thus the upper limb of the attenuator is formed by R9, R10, R13, R14, and VR5, and the amplifier input resistors R2 and R6. The lower limb of the attenuator consists of R4 from the summing junction of the amplifier to the zero volt line through SE2. SE1 connects the neon N3 to the zero volt line to provide a decimal point between the second and third digits of the display.

c) The 100 volt range is selected by SF. This connects the input signal to the input attenuator at R8, and the upper limb of the attenuator consists of R8, R9, R10, R13, R14, and VR5 in series. The lower limb of the attenuator consists of R16 and VR3 in series. The attenuated signal is connected from the junction of VR5 and R16 through SA2, SC4 and R19, to the input

of the amplifier. SF3 short circuits R7; SF1 connects neon N2 to the zero volt line, to provide a decimal point between the third and fourth digits of the display.

d) The 1000 volt range is selected by SG. The input signal is connected through SG2 to the top end of the attenuator, and the upper limb of the attenuator is as for the 100 volt range. The lower limb of the attenuator, selected by SG4, consists of R17 and VR4. The attenuated signal, taken from the junction of VR5 and R17, is connected to the amplifier through SA2, SC4, R19 and R7.

The calibration potentiometer VR2 is connected from the zero volt line to the charging current stage in the voltage-to-number converter. When 'Set 912' is selected, this control adjusts the charging current to provide an indication of 912.

The 'Set 005' potentiometer is connected between potentials of approximately ±0·8V, derived from the +15V and −20V stabilised lines through a potential divider R21, R22, R23, and R24 in the power supply. When 'Set 005' is selected, a small adjustable offset voltage is taken from the potentiometer to the summing junction of the amplifier. This offset voltage is set to obtain a reading of 005 on the digital display.

The most significant digit of the display will either show blank or 1. This is controlled by the pnp/npn pair VT1 and VT2. At the commencement of each digitising cycle, the emitter of VT2 is open circuit by the reset transistor VT2 in the voltage-to-number converter. Thus, the collector of VT2 moves positive towards a potential determined by the potential divider R5, R6. VT1 and VT2 are then cut off, with the base and emitter of VT1 at +4·7V. A positive-going carry signal from the most significant decade of the counter will be coupled through C1 to the base of VT2, which will conduct, causing the neon, N1, to strike and provide a figure 1 in the first window of the display. The collector of VT2 will move negative towards zero volts, reducing the base potential of VT1 below +4·7V. VT1 will then conduct, holding the base of VT2 positive of its emitter.

The change in potential at the base of VT1 provides an enable signal to a two input AND gate operating on logic '0' signals. The second input to this AND gate is taken from the third decade of the counter and will move negative when the count reaches 1. Thus, when the display shows 1100, both inputs to the AND gate are at zero volts, providing a signal to reset the bistable in the voltage-to-number converter, inhibiting its operation.

The Operational Amplifier Circuit

The operational amplifier circuit is shown in Fig. 4. The input signal voltage from the attenuator is coupled through R2 and R6 to the summing junction of the amplifier; noise and hum filtering is provided by C2. The offset voltage is fed to the summing junction through R1 and R3; C1 provides noise and hum filtering. The input and offset signals are summed with an overall feedback signal through R8, and on the 10 volt range, R4, connected to zero volts, provides the lower limb of the input attenuator.

The summing junction signal is chopped by VT1 which is alternately saturated and cut off at 100Hz by a chopper drive signal on its base, taken from VT8 in the power supplies. The resultant a.c. signal is coupled through C3 to the input of a three stage amplifier. The coupling diode MR1 will conduct during the negative half of the chopper waveform and will be cut off during the positive half cycle. MR2 will conduct if the summing junction is more than approximately 0·5V negative, protecting the input amplifier from gate/source breakdown.

The first stage of the input amplifier employs an F.E.T., VT2, to provide a high input impedance and low impedance drive to the second amplifying stage, VT3. This in turn controls a current amplifier VT4 driving an emitter follower VT5. The emitter volts of VT4 and the collector volts of VT5 are held constant by zener diode MR3.

DC negative feedback is taken from the emitter of VT5 to the gate of VT2 through R14 and R9, decoupled by C4 in series with R11. This feedback stabilises the d.c. operating conditions of the amplifier.

The output signal at the emitter of VT5 is coupled through R17 and C7 to the second chopper transistor VT6. This is driven between cut off and saturation at 100Hz by the chopper signal from VT8 in the power supplies. MR4 will conduct when the chopper signal tends to go positive, and VT6 will conduct on the negative half-cycles, producing a unidirectional signal, negative-going for a positive input, which is smoothed by R18 and C8, C9 in series.

The rectified and smoothed d.c. signal is further amplified, with phase inversion, in the emitter coupled differential amplifier VT7, VT8. VT8 is biassed slightly negative, to balance the negative-going input signal at the base of VT7. The output taken from the collector of VT7 drives the output stage of the amplifier VT9. Overall negative feedback is taken from the collector of VT9 to the summing junction through R8, giving the amplifier an overall gain of unity.

The output from the operational amplifier drives a buffer stage consisting of an integrated circuit operational amplifier with differential input. The phase inverted output drives

the charging current stage of the voltage-to-number converter and negative feedback, proportional to the charging current, is fed back to the second input of the integrated circuit. The calibration potentiometer VR2, on the switch and neon board, adjusts the charging current by varying the resistance across which the feedback is developed.

Voltage-to-Number Converter (Patent No. 27898/67)

The voltage-to-number converter, the circuit of which is shown in Fig. 5., contains two timing circuits having identical configurations. These two circuits are coupled electrically and thermally so that any drifts introduced into one must also appear in the other. One of these timing circuits determines the gating time, while the other provides the conversion from voltage to frequency, the two together being a voltage-to-number converter. Considering the circuit which generates the timing waveform, this consists of transistors VT7, VT9, VT11, VT12, and the associated components. VT7 is a constant current generator which will charge C8 linearly. The rising voltage across C8 will be coupled through MR2 to the emitter of VT11. VT11 and VT12 form a pnp/npn pair which are cut off during the charging period. When the emitter potential of VT11 rises to its base potential, the two transistors will switch regeneratively to a conducting state and discharge C8. The magnitude of current drawn causes the potential at the emitter and the base of VT11 to drop rapidly; the base then recovers to its normal potential determined by the zener diode MR5.

The current through the pair causes a positive voltage step across R25 which is coupled to the base of VT9, causing this transistor to conduct and so providing a second discharge path for C8 through R19 and VT9.

The transistors VT6, VT8, VT10 and the zener diodes MR1 and MR3 provide the stable reference voltage from which VT7 draws its charging current. The reference voltage is developed across MR1, and for stability, the current in this zener is held constant by VT8, R16 and MR3. MR3 operates at near constant current controlled by the transistor VT10 which has its base referred to the stable reference potential across MR1. This reference voltage is developed across R17 to give an accurate reference current into C8. The base emitter potentials of VT6 and VT7 are equal and self-compensating to temperature changes. Resistors R14, R15 across zener diode MR1 provide the calibration voltage to the switch and neon circuit.

The second timing circuit is similar in most respects to that already described;the timing capacitor C10 is charged through VT17 and the charging current is determined by the signal voltage applied to the base of VT16 from the buffer amplifier. To ensure linearity, the transistors VT16 and VT17 are included in the buffer amplifier feedback loop, the feedback signal being taken across R31 and R33 in parallel.

The pnp/npn pair which switches the circuit is VT13 and VT14, while the discharge transistor is VT15 in series with R30. The variable resistor VR2 alters the magnitude of the discharging current and enables the voltage-to-number relationship of the circuit to be linearised. Output pulses are taken from the junction of C10 and L1 through the capacitor C11 to drive the three decade counters.

The gating circuit consists of VT4 and VT5, a pnp/npn pair. It is switched by pulses from the timebase generator, the display timer, and the overload circuit. During the display period, the pnp/npn pair is cut off and the collector of VT5 moves positive towards zero volts. This potential is coupled through R20, MR4 and R29, MR6 to the pnp/npn pairs in the two timing circuits. This holds both pairs conducting so that the timing capacitors are discharged.

At the end of the display period, a positive pulse is coupled to the base of VT5, causing VT4 and VT5 to switch regeneratively to a conducting state. The collector of VT5 falls to near −20V, reverse biassing MR4 and MR6. The two timing pnp/npn pairs cut off and the voltage-to-number conversion commences.

At the end of the voltage-to-number conversion, C8 is discharged, giving a fall in potential at the collector of VT7. This negative-going waveform is coupled through C7 to the collector of VT4, cutting off VT4 and VT5. The display is then stationary until the end of the display cycle. If the voltage measured is greater than the selected range, an overload signal will be generated in the decade counter at 1100. This overload signal is fed to the base of VT3, causing a positive-going signal which is coupled through C3 to the emitter of VT5. This switches the pnp/npn pair to cut off, terminating the voltage-to-number conversion.

The timing generator consists of a unijunction transistor VT1, with its associated components. At the end of the display period, VT1 is cut off and C1 is fully discharged. C1 will then commence to charge through R2 towards an aiming potential determined by the setting of the display time control, VR1. As the emitter of VT1 approaches the upper threshold voltage, the impedance between b2 and b1 will fall and emitter current will be drawn to discharge C1. When the emitter falls to the lower threshold voltage, the impedance from b2 to b1 will rise, and the cycle will recommence.

The current drawn through R3 as VT1 conducts will provide a negative pulse which is coupled through C2 to the base of VT2, cutting it off. This provides a reset pulse to the decade

counters and the '1' display bistable. As VT1 cuts off, the rise in potential at b2 provides a positive switching edge through C5 to switch on VT4 and VT5.

When the display timer control is switched to 'Hold', the emitter circuit of VT1 is open circuited, inhibiting operation of the display timing circuit.

The Decade Counter Board (Patent No. 27897/67)

The decade counter consists of a series of pnp/npn pairs connected in cascade as a 'ripple-through' counter. In each case, the npn transistor of the pair is also used as the driver transistor for the particular number cathode of the neon indicator tube. Thus, a simple circuit has been obtained using low cost components and no diode decoding matrices are required.

The circuit schematic of the decade board is shown in Fig. 7. Since the circuits of most of the pnp/npn pairs are identical, the operation of the first, second, and last only will be described.

The counter is reset by the monostable circuit VT1, VT2. The emitter of VT1 is returned to zero volts through transistor VT2 on the voltage-to-number conversion circuit. This transistor is normally conducting, and is cut off when reset is required. This cuts off VT1, causing its collector to move positive towards 4·7V, so that the base of VT2 moves positive and VT2 conducts in saturation. This causes the 'drive input 2' line to move negative to +0·5V, and therefore cuts off all the npn/pnp pairs. These are held off long enough for all the time constants throughout the chain to discharge.

At the end of the reset period, when VT1 returns to conduction, VT2 will be cut off and the 'drive input 2' line will move positive towards 4·7V. The bases of all pnp transistors in the counting chain, with the exception of VT3, will be at +4·7V. The base of VT3, however, is held at a potential between 4·7V and zero volts by the potential divider R6, R7. Thus, VT3 will conduct, switching on VT4 in saturation. The neon indicator will then show zero and the potential of the emitter of VT3 will be half a volt positive of its base potential.

When a negative-going trigger signal is applied to the counter on the 'drive input 2' line, the monostable triggers, causing the emitter of VT3 to move negative below its base potential, cutting off VT3 and VT4. The collector of VT4 will then move positive. The positive-going signal at the collector of VT4 is coupled through C3 and R11 to the base of VT6, which commences to conduct in saturation, causing the figure 1 to show on the neon indicator. The collector potential of VT6 then falls to approximately +0·5V and as the monostable resets, VT5 comes into conduction, holding the base of VT6 positive so that the circuit conducts. Except during the reset pulse, the time constant of the monostable is determined by C2, R3, and is too short for the coupling time constants through the counter to discharge.

The next negative-going input signal on 'drive input 2' will cause a similar sequence. The emitter of VT5 is driven negative by the monostable and ceases to conduct, so that its collector and the base of VT6 move negative towards −4·7V. This cuts off VT6 and its collector moves positive, conveying a trigger signal to the next pnp/npn pair.

Successive trigger signals on the 'drive input 2' line will cause the energised pair to ripple through the counter until the 9 stage is reached. When the 9 stage is cut off by the monostable, the resultant positive-going signal from the base of VT21 is used as a carry propagate signal for the next counter. The carry signals are fed into the ensuing decade on 'drive input 1' causing the monostable to change state.

Thus, the least significant decade receives input signals on 'drive input 2' from the voltage-to-number converter, while the other two decades receive carry signals from the previous decade on 'drive input1'. The carry output from the most significant decade operates a bistable circuit to bring up a 1 in the most significant window. The diodes MR11-19 are provided to protect the switching transistors from base-emitter breakdown.

The Power Supplies

The power supplies for the digital voltmeter, shown in Fig. 9., follow a fairly conventional pattern. The mains transformer primary is tapped for working at 240V, 220V, 115V, or 110V. A 0-225V secondary is half-wave rectified by MR3 into the reservoir capacitor C1. This gives a 257V line for the neon display tubes; a +75V line, also required for the neon display tubes, is developed from the 257V line through R3 and the zener diode MR7.

The centre-tapped 28V secondary feeds two full-wave rectifier circuits, one giving a +15V supply through MR4 and MR5, smoothed by R2 and C2, and the other giving a −20V supply through MR1 and MR2, smoothed by C3. A diode, MR6, is connected in series with the smoothing capacitor C2 and generates a rectangular waveform from the charging current at 100Hz to provide the chopper drive voltage for the input amplifier. This waveform is amplified and squared by VT8 which draws its collector current from −20V through R25. A zener stabilised line at +4·7V is obtained across MR8 in series with R4 from +15V to 0V.

The +15V line is drawn through the series stabilising transistor VT3. This is controlled by a single stage amplifier VT5 which is referred to the zener diode MR13 and receives error signals from the +15V rail through the potentiometer R16, R17. VT1 is a constant current transistor, the base potential of which is stabilised by the zener diode MR10. This transistor provides a high dynamic load for VT5 to give the maximum effective gain.

The stabilising circuit for the −20V supply is similar, but includes two series stabilising stages to carry the extra current. The amplifier stage VT7 is referred to the zener diode MR14, and receives error signals from the −20V line through the potentiometer R19, R20. The constant current transistor VT2 provides a high dynamic load for VT7; its base potential is stabilised by the zener diode MR11. A −4·7V zener stabilised supply is obtained from MR9 in series with R5 from −20V to 0V.

5. MAINTENANCE

General

The information provided in this section will assist in locating faults should they develop; it also gives the correct method for assembling and removing printed circuit boards from the instrument. The setting-up procedure will enable the customer to recalibrate his instrument after corrective maintenance.

All the sub-assemblies within the instrument are replaceable, and Weir Electronics Limited offer a replacement service as the most rapid means of instrument repair.

Dismantling Procedure

a) Turn the instrument upside down; extract the four screws holding the case to the base plate. Turn the instrument right side up and move the carrying handle/tilt stand up to the top of the case; carefully lift off the top case assembly.

b) Undo the two 2BA nuts below the attenuator assembly.

c) Undo the two screws holding the mains transformer to the base plate. Lift and work back from the front panel the assembly of printed circuit boards.

d) With the boards out of the case, the instrument will work with full access for simplified fault finding. The three decade boards are interchangeable and this assists in isolating faults.

e) The unit may be reassembled in its case by reversing the above procedure.

NOTE: On no account should the printed circuit sockets be strained sideways, e.g., by removing or inserting decade boards while the rest of the assembly is in the case. A sideways strain is liable to result in intermittent contact.

Setting-up Procedure

1. The setting-up procedure given here describes the steps required to adjust the preset controls of the instrument. The equipment required to perform these tests consists of one accurate digital voltmeter (0·05% or better) and stable power supplies providing up to 1000 volts. An attenuator may also be required to obtain voltages below one volt.
2. Switch on the instrument and allow thirty minutes for it to reach thermal stability.
3. If corrective maintenance has been carried out on the reference voltage circuits, or a new amplifier board has been fitted, the reference voltage will probably have changed from that shown on the front panel label. The voltage must therefore be checked and a new label fitted, if necessary.
4. To measure the reference voltage, proceed as follows:
   Connect an accurate digital voltmeter (0·05% or better) from the reference voltage line (Point A on Fig. 6) to the negative input terminal. Press the 'cal' button; the reading should be between 0·800 and 1·060V. If it differs from the figure shown on the front panel label, a new label marked with the new reference voltage should be fitted.
5. Connect a stable supply, with attenuators if necessary, to deliver voltages from 5mV to 1·1V. Set the supply to deliver 5mV and adjust the 'Set 005' preset until the digital display shows 005.
6. Set the input voltage to 300mV and adjust the 'Set 912' calibration control until the digital display shows 300.
7. Set the input voltage to 1V and adjust the 'linearity' control at the rear of the amplifier board until the digital display shows 1·000.
8. Repeat 5, 6, and 7 to confirm the settings of the 'Set 005', 'Set 912' and 'linearity' controls. If further adjustments are required, 8 may be repeated.

9. Press the 'Set 005' button and, if necessary, modify the value of R39 until the digital display shows 005. This resistor is selected on test; after corrective maintenance, a different value may be required.

10. Press the 'Set 912' button and adjust the 'Set 912' control until the digital display shows the reference voltage measured in 4.

11. Set the input voltage at various levels between 0 and 1 volt and verify the linearity of the digital conversion. The 1 volt range is now correctly set up.

12. Set the input voltage to 10V; select the 10V range on the instrument and adjust VR5 until the digital display shows 10·00.

13. Set the input voltage to 100V; select the 100V range on the instrument and adjust VR3 until the digital display shows 100·0.

14. Set the input voltage to 1000V; select the 1000V range on the instrument and adjust VR4 until the digital display shows 1000.

15. The three preset potentiometers are mounted on the attenuator assembly and are clearly marked 'Set 1000V, 100V, and 10V'.

Fault Finding Procedures

The following tests will assist in identifying the printed circuit board on which a fault has occurred:-

1. Power Supplies

Check all power supplies and verify that the measured voltage lies within the limits shown in the following table. The monitor points listed are shown on the Component Location Diagrams.

Monitor Point	Nominal Voltage	Tolerance
B	+15V	±7%
C	−20V	±7%
D	+4·7V	±7%
E	−4·7V	±7%
F	+75V	±7%
G	257V	Nominal

2. Amplifier Chopper Waveform

The normal chopper waveform, which may be examined at point H, is shown in Fig. 6; any material deviation from this waveform will indicate an amplifier fault condition.

A positive excursion, several times larger than the negative excursion, indicates an offset error.

A very large positive excursion indicates a break in the amplifier feedback system.

A negative excursion will indicate a negative input signal.

3. Table of Faults

Fault	Action
Inaccurate readings, all ranges.	1. Check 'Set 005' and 'Set 912' settings. 2. Check setting of 'linearity' control. 3. Check amplifier chopper waveform. 4. If the above tests fail to correct the error, check the power supply lines. 5. If power supply lines are correct, amplifier or V/N converter is faulty; obtain replacement board.
Inaccurate readings, one range.	1. Check setting of relevant range potentiometer. 2. Check attenuator resistor specific to that range.
Continuously cycling display.	1. Fault will probably be in gating circuits of V/N converter; obtain replacement board.
Incorrect display.	1. A faulty decade board will spoil the display on all decades greater than the faulty board. Move the suspect board to another position to confirm the fault. Obtain and fit a replacement board.

6. PARTS LIST

The following list includes all replacement parts with circuit references, values and tolerances, where applicable, and part numbers. When ordering, please quote the NAME, TYPE, and SERIAL NUMBER of the instrument, together with the CIRCUIT REFERENCE and the DESCRIPTION of PART.

Circuit Ref.	Description	Value	Rating	Tol.	Part No.
Switch and Neon Assembly					
R1, 4	Resistor C.F.	100k	½W	5%	471-1-100k
R2	Resistor C.F.	1k	½W	5%	471-1-1k
R3	Resistor C.F.	10k	½W	5%	471-1-10k
R5	Resistor C.F.	120k	½W	5%	471-1-120k
R6, 18	Resistor C.F.	430k	½W	5%	471-1-430k
R20, 21	Resistor C.F.	100	½W	5%	471-1-100
C1	Capacitor	360pF	125V		Suflex HS
C2	Capacitor	82pF	350V	2%	Lemco 316
VT1	Transistor				Mullard BCY 72
VT2	Transistor				Fairchild C407
MR1	Silicon Diode				Texas 1N660
N1	Neon				Hivac 23L
N2, 3, 4, 5, 6	Neon				R.G.F. Elect. MN500
Pre-attenuator P.C.B.					
R7 *	Resistor M.F.	101k		1%	473-1-101k
R8 *	Resistor M.F.	1M		1%	473-1-1M
R9, 10, 13, 14 *	Resistor M.F.	2·2M		1%	Morganite FC70
R16 *	Resistor M.F.	99k		1%	473-1-99k
R17 *	Resistor M.F.	9·8k		1%	473-1-9·8k
VR3	Preset Pot.	5k			Iskra PN-10B
VR4	Preset Pot.	500			Iskra PN-10B
VR5	Preset Pot.	500k			Iskra PN-10B
Cal and Switch P.C.B.					
R11	Resistor M.F.	1M	½W	2%	Electrosil C5
R12	Resistor M.F.	5·1k	½W	2%	Electrosil C5
R19 *	Resistor M.F.	320k		1%	Morganite FC70
C3	Capacitor	10,000pF	1000V	20%	Waycom MAIL611
Cal and Switch					
VR1, 2	Trim Pot.	1k		5%	M.E.C. Ltd. MF32
Amplifier					
R1, 3	Resistor C.F.	5·6M	½W		471-1-5M6
R2 *	Resistor M.F.	320k	1W	1%	Morganite FC70
R4 *	Resistor M.F.	1·09M		1%	Welwyn 4015
R5, 16, 17, 20, 26	Resistor C.F.	10k	½W		471-1-10k
R6 *	Resistor M.F.	259k	1W	1%	Morganite FC70
R7	Resistor C.F	2·2k	½W		471-1-2k2
R8 *	Resistor M.F.	1M		1%	473-1-1M
R9	Resistor C.F.	2·2M	½W		471-1-2M2
R10	Resistor C.F.	22k	½W		471-1-22k
R11	Resistor C.F.	470	½W		471-1-470
R12	Resistor C.F.	8·2k	½W		471-1-8k2
R13	Resistor C.F.	2·7k	½W		471-1-2k7
R14, 22	Resistor C.F.	1M	½W		471-1-1M
R15	Resistor C.F.	18k	½W		471-1-18k
R18	Resistor C.F.	4·7k	½W		471-1-4k7
R19, 23	Resistor C.F.	1k	½W		471-1-1k
R21	Resistor C.F.	100k	½W		471-1-100k

Circuit Ref.	Description	Value	Rating	Tol.	Part No.
Amplifier Cont.					
R24	Resistor C.F.	820	½W		471-1-820
R25	Resistor C.F.	120k	½W		471-1-120k
R27	Resistor C.F.	240	½W		471-1-240
R28	Resistor C.F.	5·1	½W		471-1-5·1
R29	Resistor C.F.	12k	½W		471-1-12k
C1	Capacitor	0·01μF	100V		S.T.C. PMA0·01M100
C2	Capacitor	0·1μF	250V		S.T.C. PMA0·1M250
C3	Capacitor	0·047μF	100V		S.T.C. PMA0·047M100
C4	Capacitor El.	33μF	10V		Sprague 150D 336X9010B2
C5, 10, 11	Capacitor	0·1μF	100V		S.T.C. PMA0·1M100
C6, 14	Capacitor	0·022μF	100V		S.T.C. PMA0·022M100
C7	Capacitor	0·22μF	100V		S.T.C. PMA0·22M100
C8, 9	Capacitor El.	400μF	4V		Mullard C426ARB400
C12	Capacitor	39pF	63V		Iskra KSN2
C13	Capacitor	2·2μF	100V		S.T.C. PMA2·2M100
IC	Integrated Circuit				Motorola MC1433P
VT1	Transistor				Mullard BCY70
VT2	F.E.T.				Motorola MPF103
VT3, 5, 7, 8	Transistor				Mullard BC108
VT4, 6, 9	Transistor				Mullard BCY72
MR1, 2, 4, 6	Diode				482-2
MR3	Zener Diode		7·5V		Mullard BZY88C7V5
MR5	Zener Diode		15V		Mullard BZY94C15
V/N Converter					
R1	Resistor C.F.	3·9k	½W		471-1-3k9
R2	Resistor C.F.	470k	½W		471-1-470k
R3	Resistor C.F.	150	½W		471-1-150
R4	Resistor C.F.	390	½W		471-1-390
R5	Resistor C.F.	68k	½W		471-1-68k
R6, 7, 9	Resistor C.F.	4·7k	½W		471-1-4k7
R8	Resistor C.F.	200k	½W		471-1-220k
R10	Resistor C.F.	1·8k	½W		471-1-1k8
R11, 34	Resistor C.F.	560	½W		471-1-560
R12, 18, 35	Resistor C.F.	22	½W		471-1-22
R13	Resistor C.F.	130k	½W		471-1-130k
R14 *	Resistor M.F.	27k		1%	473-1-27k
R15 *	Resistor M.F.	5·6k		1%	473-1-5k6
R16	Resistor M.F.	820	½W	2%	Electrosil C5
R17 *	Resistor M.F.	39k		1%	473-1-39k
R19, 30	Resistor C.F.	10	½W		471-1-10
R20, 29	Resistor C.F.	47k	½W		471-1-47k
R21, 24, 26	Resistor C.F.	1k	½W		471-1-1k
R22, 28	Resistor C.F.	100k	½W		471-1-100k
R23	Resistor C.F.	1M	½W		471-1-1M
R25, 27	Resistor C.F.	2·2k	½W		471-1-2k2
R31 *	Resistor M.F.	180		1%	473-1-180
R36, 37	Resistor C.F.	100	½W		471-1-100
R38	Resistor C.F.	150	½W		471-1-150
VR1	Potentiometer	10k			Egen 415G
VR2	Potentiometer	25			Welwyn P25
C1	Capacitor	2·2μF	100V		S.T.C. PMA2·2M100
C2	Capacitor El.	1·6μF	25V		Mullard C426ASF16
C3	Capacitor	0·022μF	100V		S.T.C. PMA0·022M100
C4	Capacitor El.	50μF	25V		Mullard C426ARF50
C5, 7	Capacitor	0·01μF	100V		S.T.C. PMA0·01M100
C6	Capacitor	390pF	160V		Iskra KSN
C8	Capacitor	2·2μF	100V	5%	S.T.C. PMA2·2J100
C9	Capacitor	0·1μF	100V		S.T.C. PMA0·1M100
C10	Capacitor	0·1μF	100V	5%	S.T.C. PMA0·1J100
C11	Capacitor	39pF	160V		Iskra KSN
L1	Inductor				A5032-22

Circuit Ref.	Description	Value	Rating	Tol.	Part No.
V/N Converter Cont.					
VT1	Unijunction				Texas TIS43
VT2, 3, 5, 10	Transistor				Mullard BC108
VT4, 8	Transistor				Mullard BCY72
VT6	Transistor				Mullard BC107
VT7, 11, 14, 16	Transistor				Mullard BCY70
VT9, 12, 13, 15, 17	Transistor				NKT10339
MR1	Zener Diode		6V	2%	Semitron ZOB6
MR2, 4, 6, 7, 8, 9, 10	Diode				482-2
MR3, 5	Zener Diode		4·7V		481-4V7-1
Decade P.C.B.					
R1	Resistor C.F.	2·2k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R2, 13, 17, 21, 25, 29, 33, 37, 41, 45	Resistor C.F.	10k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R3	Resistor C.F.	120k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R4, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46	Resistor C.F.	68k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R5, 6, 8	Resistor C.F.	1k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R7	Resistor C.F.	1·8k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R9	Resistor C.F.	22k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R11, 12, 15, 16, 19, 20, 23, 24, 27, 28, 31, 32, 35, 36, 39, 40, 43, 44	Resistor C.F.	4·7k	$\frac{1}{2}$W	5%	Piher Waycom WP051
R47	Resistor C.F.	68k	1W	5%	Piher Waycom WP11
C1	Capacitor	180pF	125V	10%	Suflex HS
C2, 4, 6, 8, 10, 12, 14, 16, 18, 20	Capacitor	82pF	350V	2%	Lemco 316
C3, 5, 7, 9, 11, 13, 15, 17, 19	Capacitor	1,000pF	125V	10%	Suflex HS
VT1, 2	Transistor				Mullard BC108
VT3	Transistor				Mullard BCY72
VT4, 6, 8, 10, 12, 14, 16, 18, 20, 22	Transistor				Fairchild C407
VT5, 7, 9, 11, 13, 15, 17, 19, 21	Transistor				Texas BCY72
MR1, 11, 12, 13 14, 15, 16, 17, 18, 19	Diode				Mullard OA91
MR2, 3, 4, 5, 6, 7, 8, 9, 10	Diode				Texas 1N660
V1	Numerical Indicator Tube				S.T.C. GN6
Power Supply					
R2	Resistor C.F.	10	$\frac{1}{2}$W	5%	471-1-10
R3	Resistor C.F.	33k	1W	5%	Piher Waycom WP11
R4	Resistor C.F.	680	1W	5%	Piher Waycom WP11
R5	Resistor C.F.	1k	1W	5%	Piher Waycom WP11
R6, 7, 8, 11	Resistor C.F.	4·7k	$\frac{1}{2}$W	5%	471-1-4k7
R9, 12, 25	Resistor C.F.	10k	$\frac{1}{2}$W	5%	471-1-10k
R10, 14, 22, 23	Resistor C.F.	1k	$\frac{1}{2}$W	5%	471-1-1k
R13	Resistor C.F.	18	$\frac{1}{2}$W	5%	471-1-18
R15	Resistor C.F.	47	$\frac{1}{2}$W	5%	471-1-47
R16, 17, 20	Resistor C.F.	2·7k		1%	Electrosil C5
R19	Resistor M.F.	4·7k		1%	Electrosil C5
R21	Resistor C.F.	18k	$\frac{1}{2}$W	5%	471-1-18k
R24	Resistor C.F.	22k	$\frac{1}{2}$W	5%	Piher Waycom WP051

Circuit Ref.	Description	Value	Rating	Tol.	Part No.
Power Supply Cont.					
C1	Capacitor El.	32μF	350V		Sprague HD2
C2, 3	Capacitor El.	250μF	64V		Mullard C437/AR/H250
C4, 5	Capacitor	0·01μF			Hunts SLM13 Type 310
C6, 7	Capacitor El.	50μF	25V		Mullard C426/AR/F50
C9, 10	Capacitor	0·1μF	250V		Mullard C281/W/100k
VT1, 6, 7	Transistor				Mullard BCY70
VT2	Transistor				Texas D1533/J301
VT3, 4	Transistor				Mullard BFY51
VT5	Transistor				Mullard BC108
VT8	Transistor				Mullard BCY72
MR1, 2, 4, 5	Diode				Thorn-A.E.I. BY125
MR3	Diode				Iskra BY237
MR6	Diode				482-2
MR7	Zener Diode				S.T.C. Z3B750CF
MR8, 9	Zener Diode				Mullard BZY88C4V7
MR10, 11, 13, 14	Zener Diode				Mullard BZY88C6V8
MR12	Diode				Mullard OA91
TX	Transformer Issue A				Hinchley C5032/55
	Fuse		250mA		Radio Spares
Connector P.C.B.					
R1	Resistor C.F.	100	$\frac{1}{2}$W	5%	471-1-100
C1, 5	Capacitor El.	200μF	10V		Mullard C426AR/D200
C2, 3, 4,	Capacitor El.	50μF	25V		Mullard C426AR/F50
MR1, 2, 3	Diode				Mullard OA91

* These components have a temperature coefficient of 50PPM/°C

Abbreviations

C.F. Carbon Film El. Electrolytic M.F. Metal Film

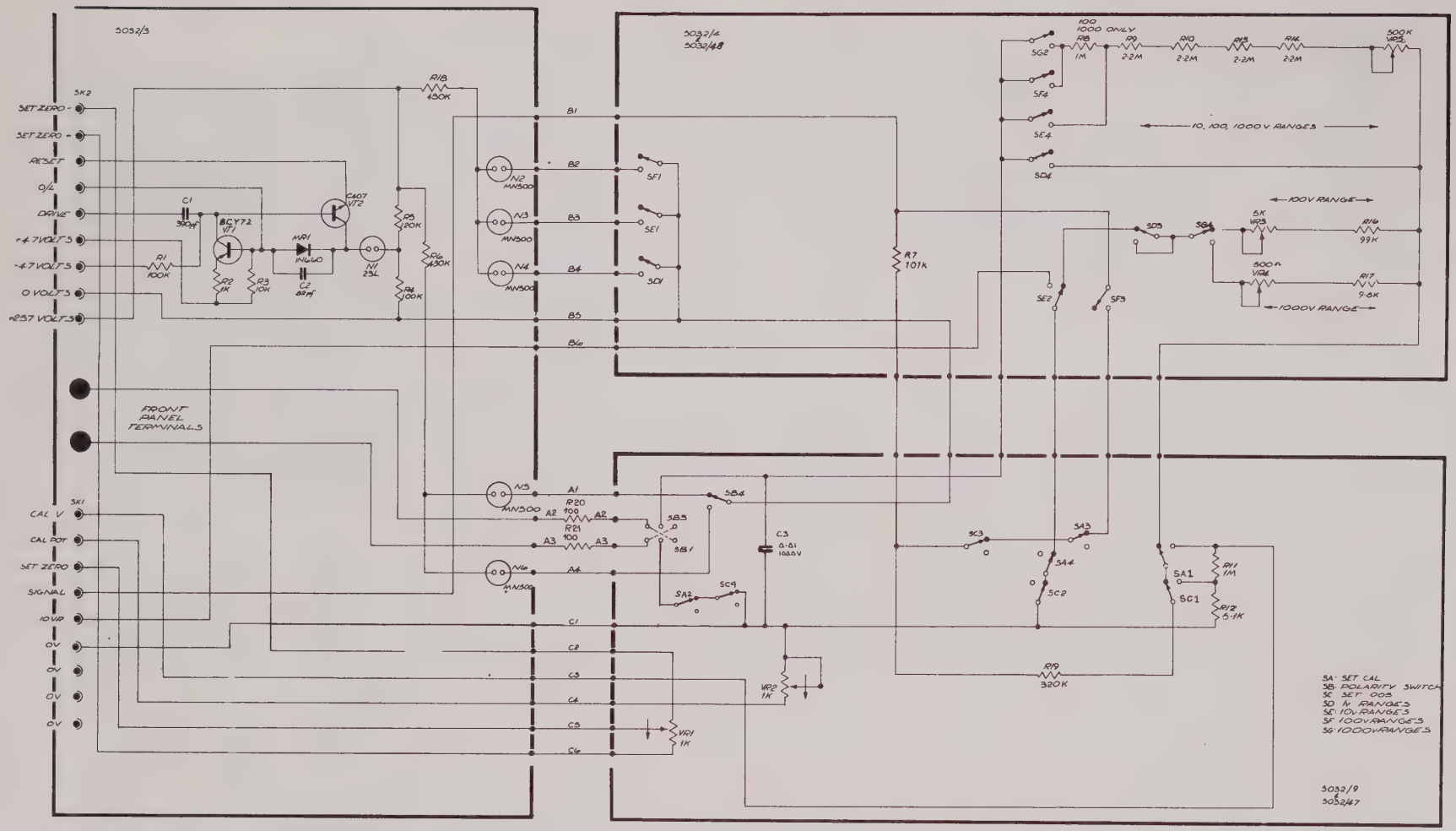
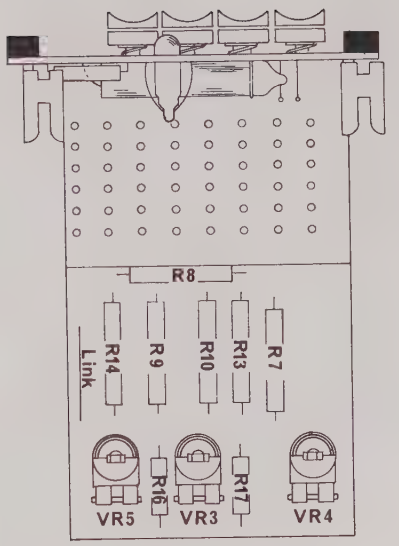
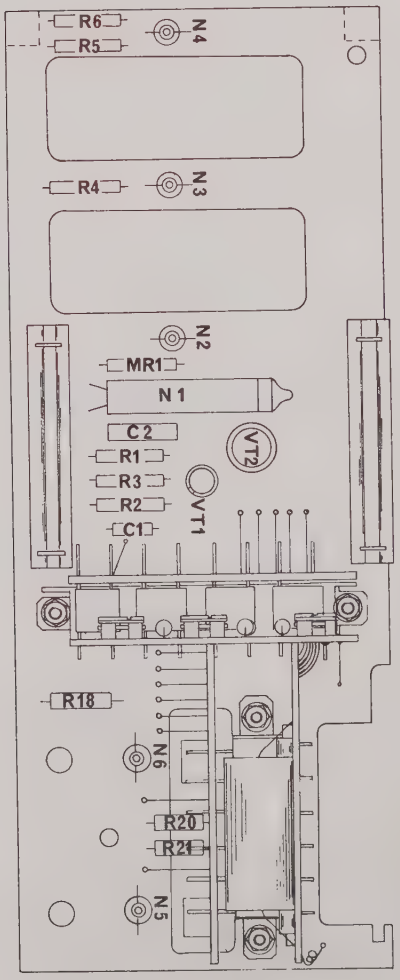


Fig. 2. Switch and Neon Circuit Diagram





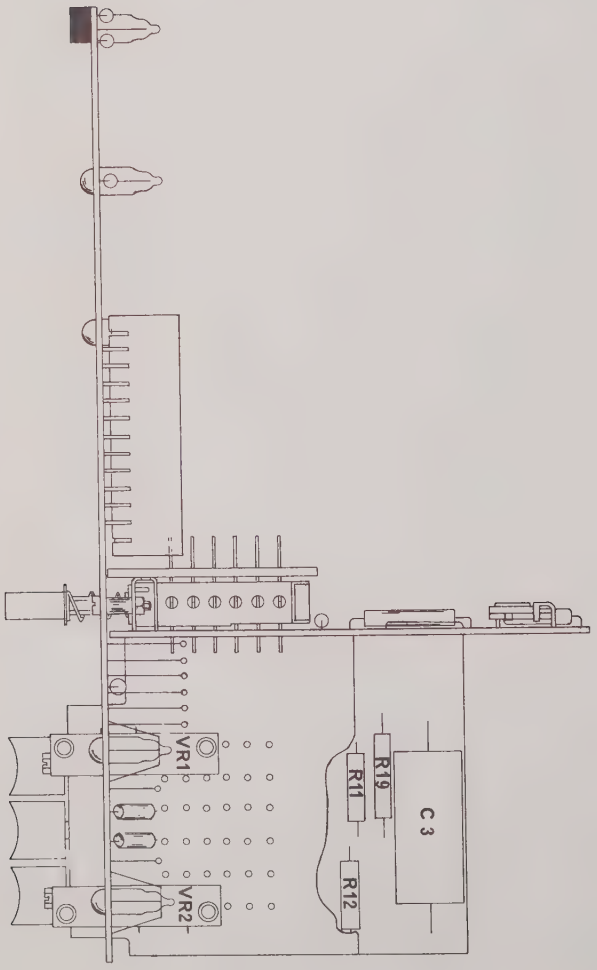


Fig. 3. Switch and Neon Layout Diagram

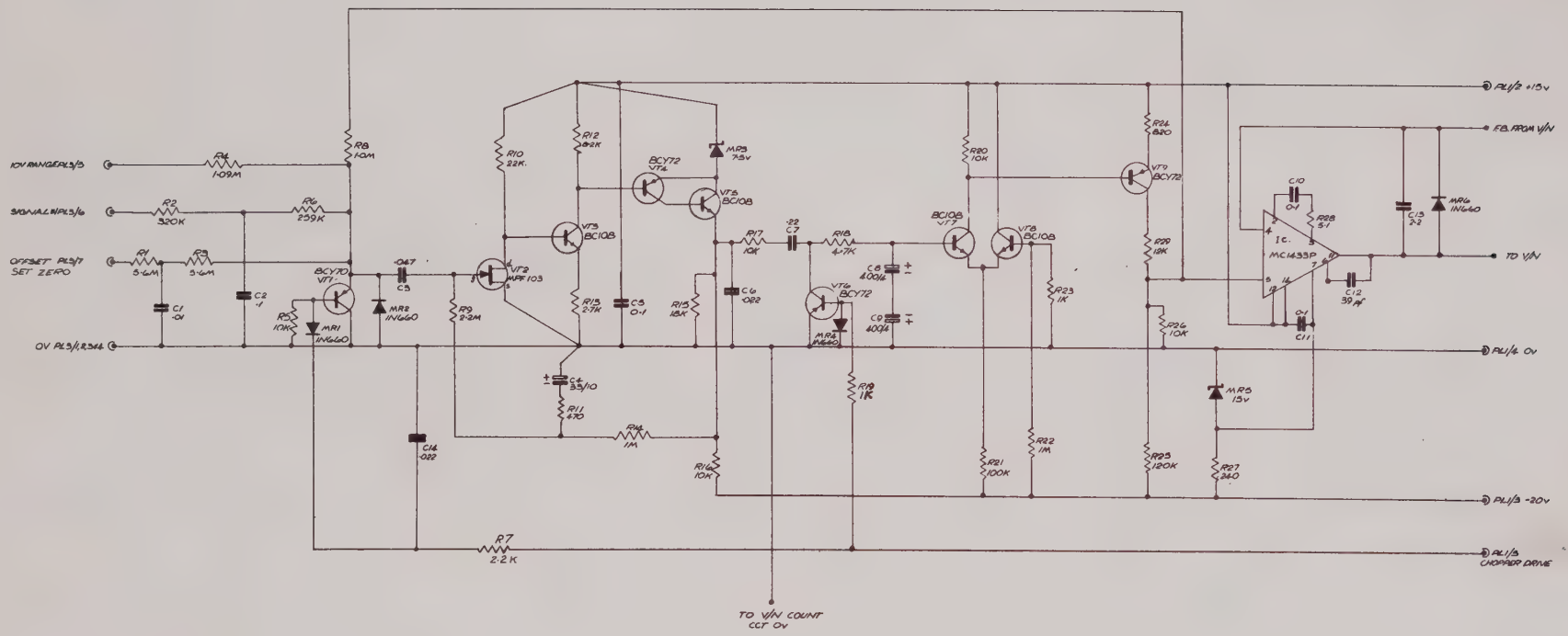


Fig. 4. Amplifier Circuit Diagram

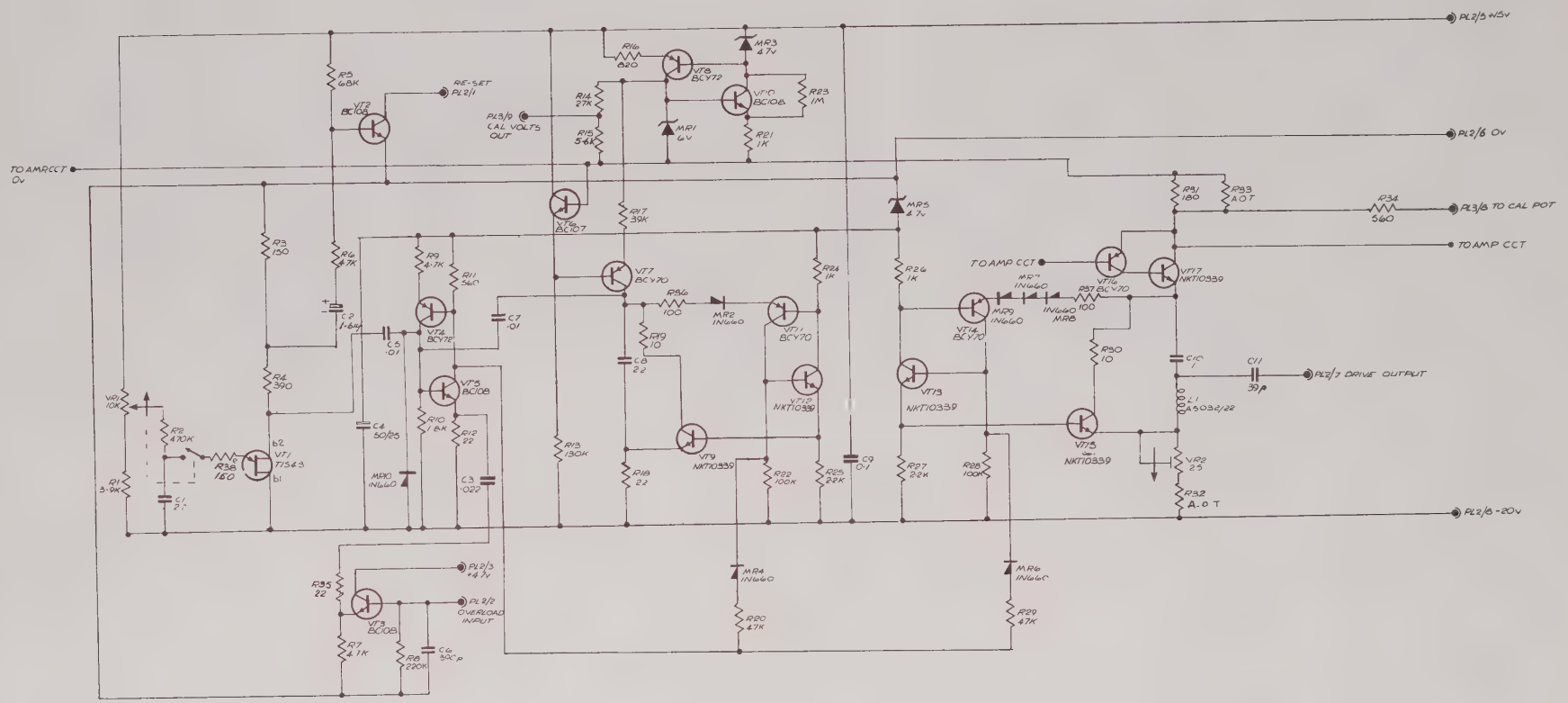


Fig. 5. V - N Converter Circuit Diagram

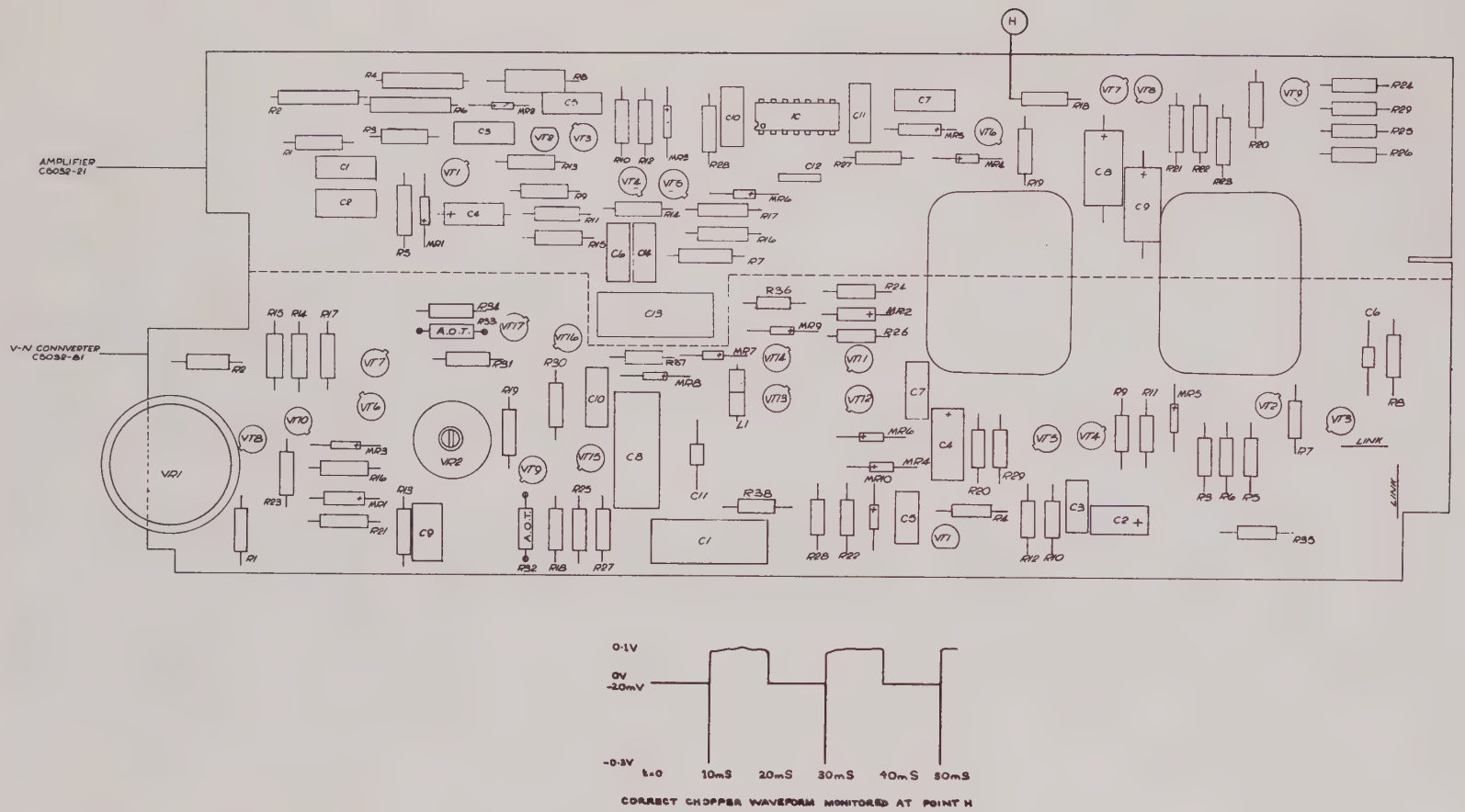


Fig. 6. Amplifier and V - N Converter Layout Diagram

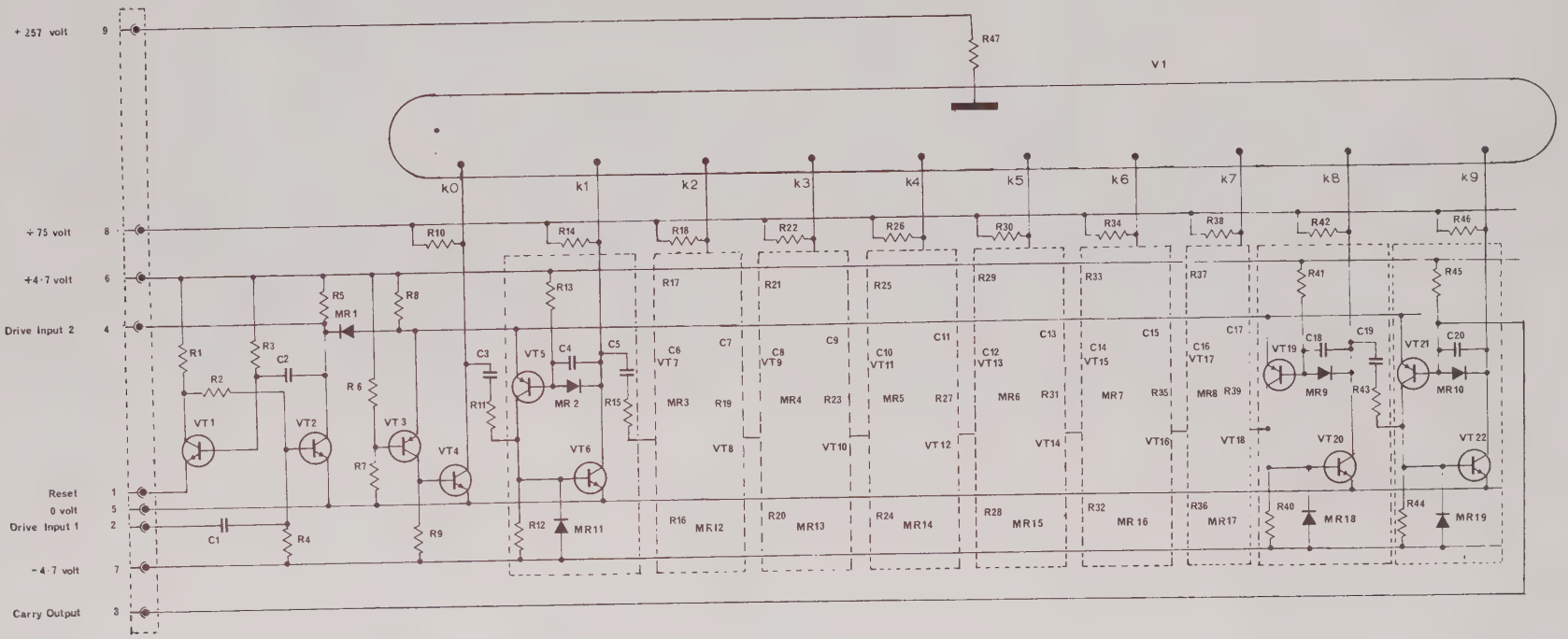


Fig.7. Decade Board Circuit Diagram

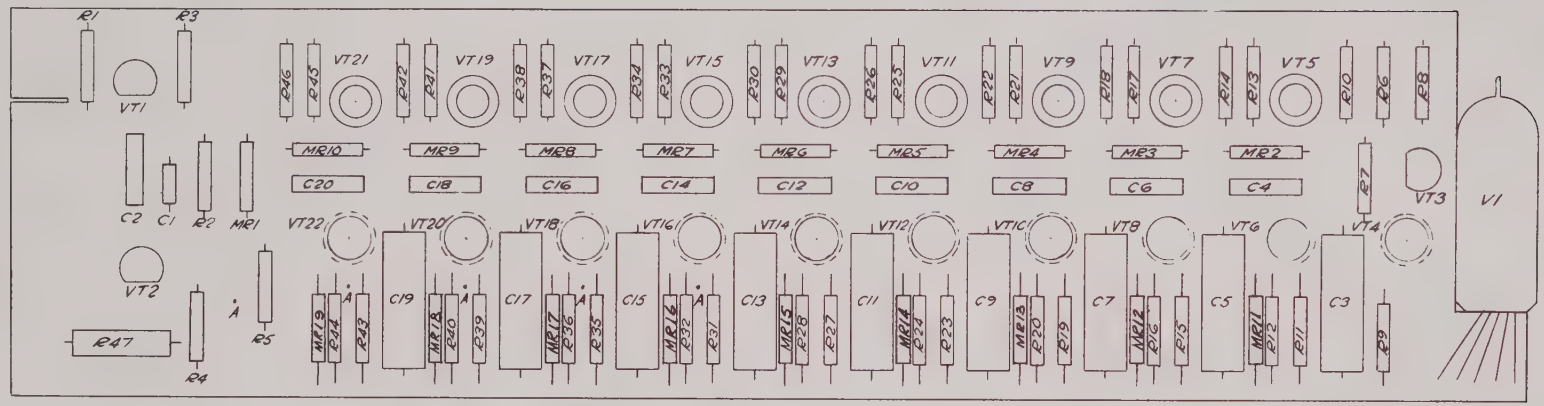


Fig. 8. Decade Board Layout Diagram

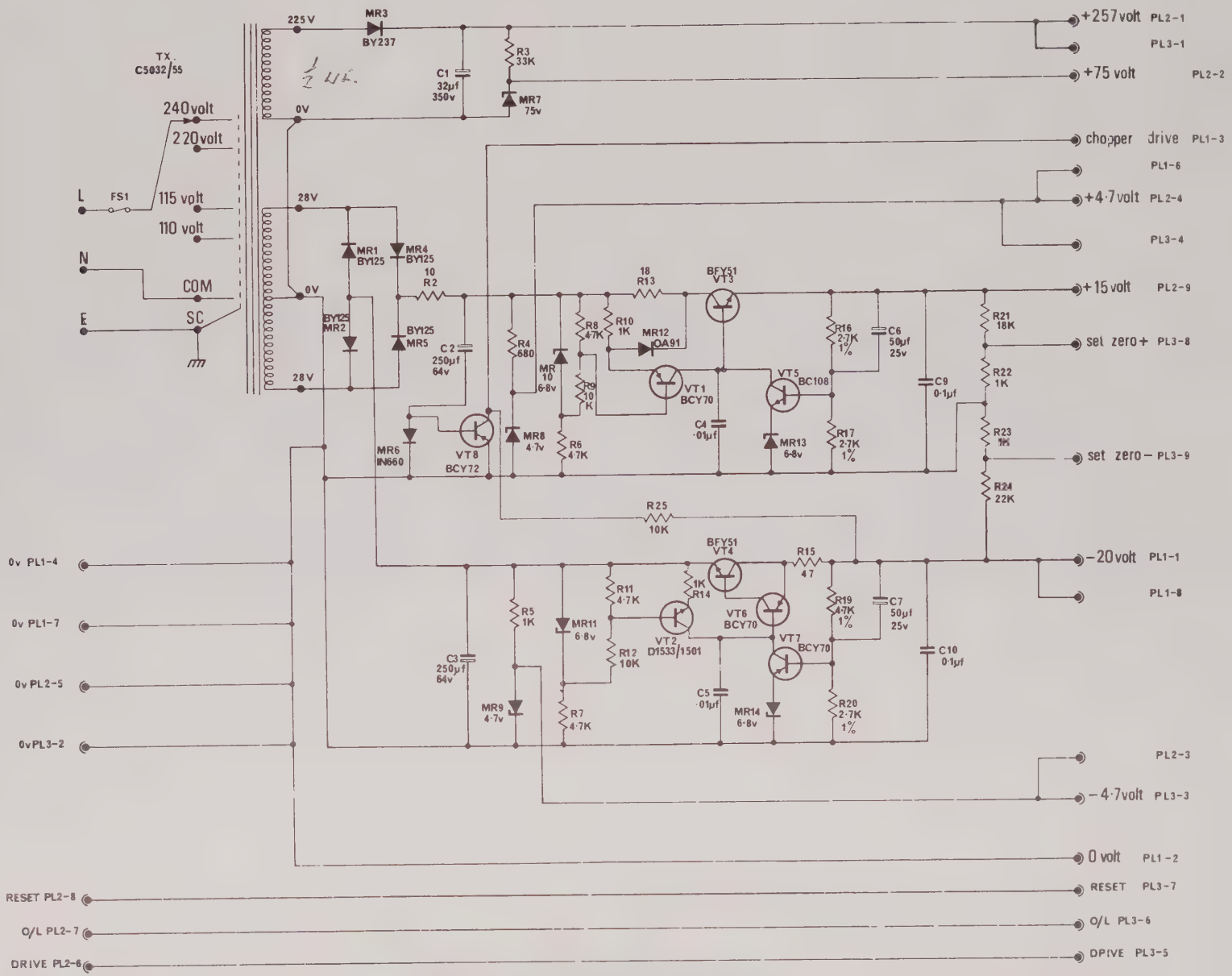


Fig. 9. Power Supplies Circuit Diagram

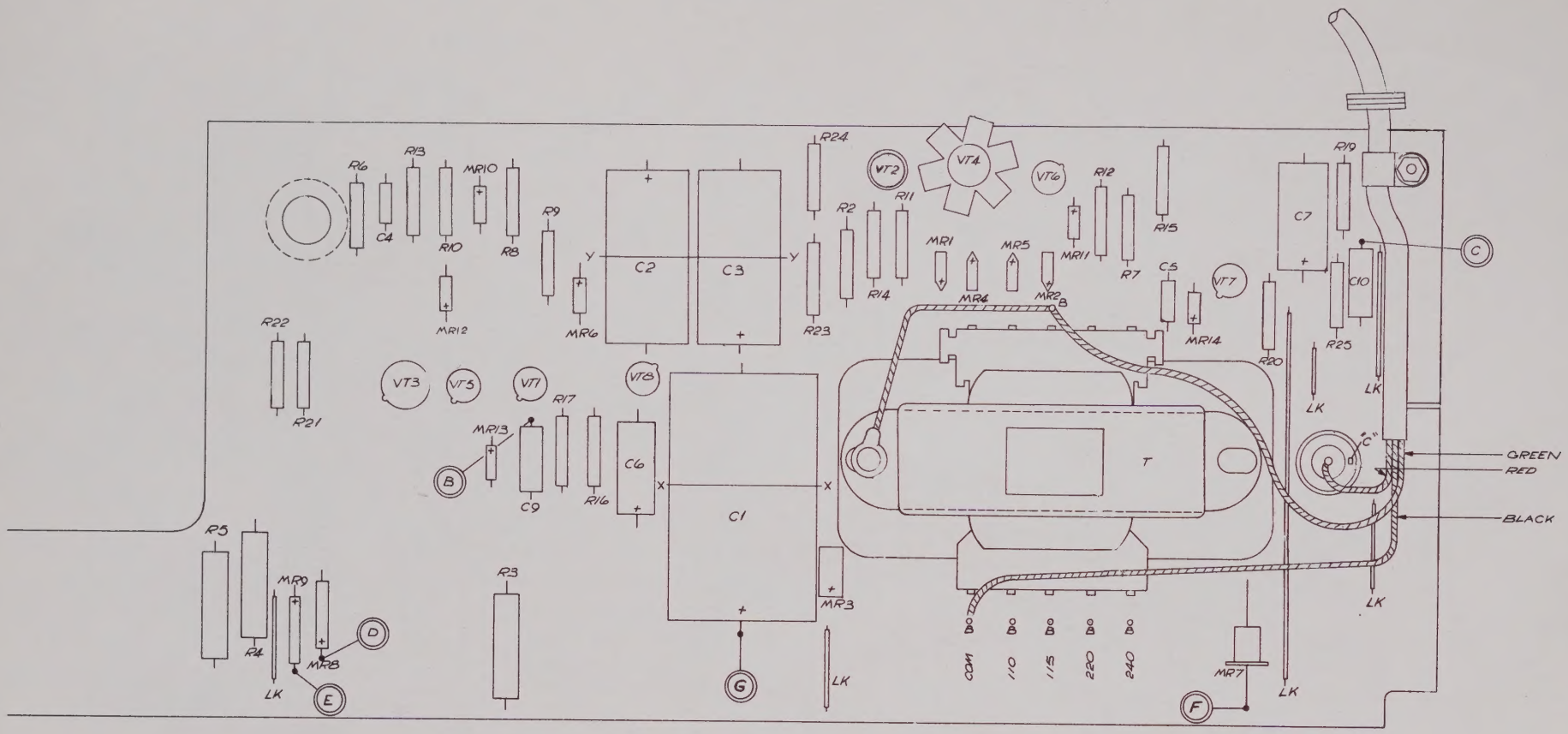


Fig. 10. Power Supplies Layout Diagram

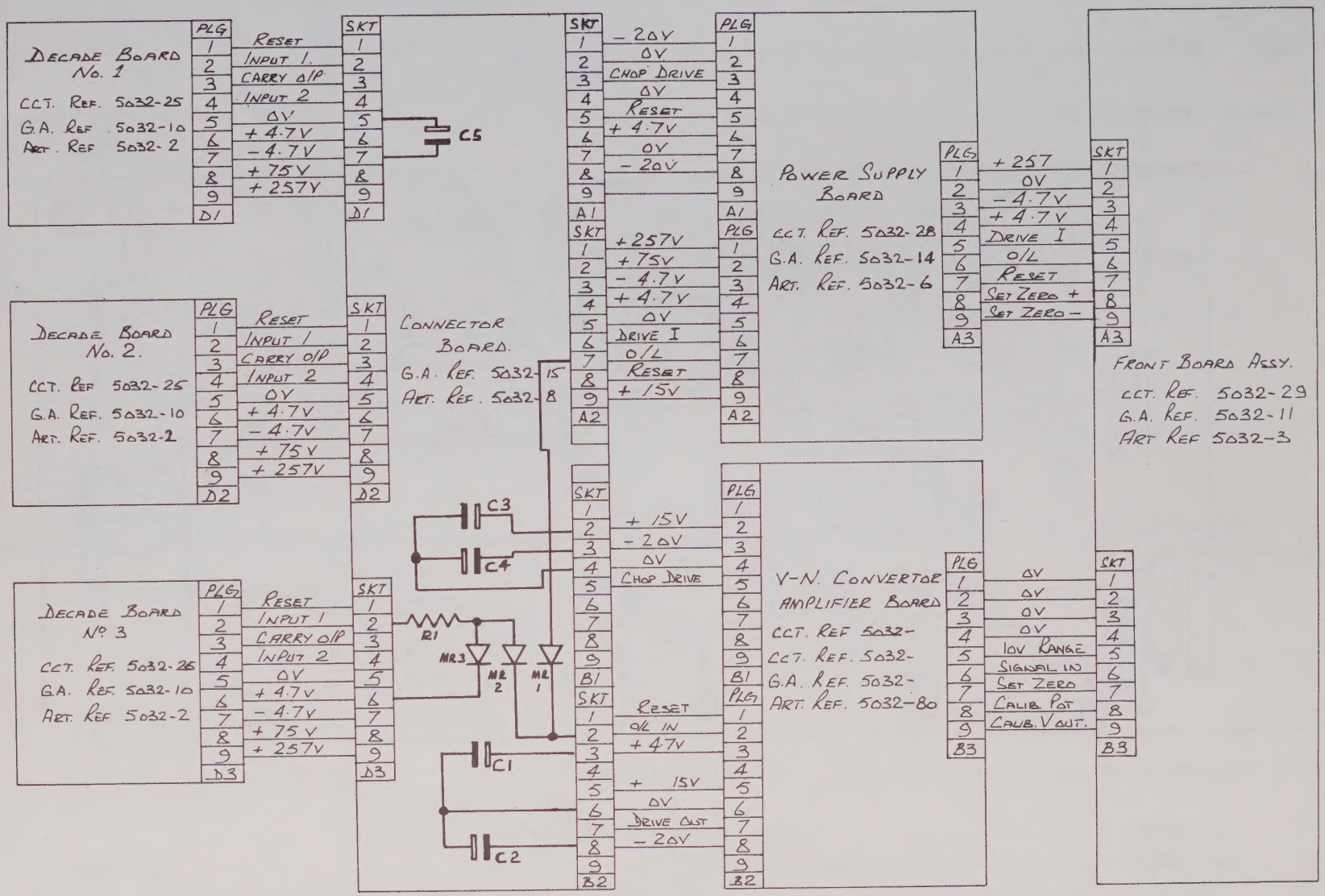


Fig. 11. Interconnection Circuit Diagram

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